ultimately from the same base claim (claim 1 or claim 2 in the alternative). Thus, the first and second embodiments are covered by generic claims 1 and 2.

Similarly, with respect to the third embodiment, this embodiment is similar to the first embodiment, except that in the third embodiment, the area of the upper electrode of the two capacitors are the same, whereas in the first embodiment, the areas are different (see the specification at page 30, lines 4-26). These features are claimed in at least claims 28 (same area) and 29 (different areas). Claims 28 and 29 both depend from the same base claim (claim 1 or claim 2 in the alternative). Thus, the first and third embodiments are covered by generic claims 1 and 2.

Accordingly, the applicant submits that first, second and third embodiments (Figs. 1-13) are not distinct species and should be examiner together. Claims 1-50 are readable on all three embodiments.

Amendment

Prior to examining the application on the merit, please amend the claims as follows:

Please replace the text of claims 1-18, 20, 22-33, 35, 36, 44, 48 and 49 with the following text:

1. A semiconductor device having a non-volatile memory transistor, comprising:

a first capacitor element and a second capacitor element,

the non-volatile memory transistor, the first and the second capacitor element being formed in one semiconductor substrate,

the first capacitor element including a first lower electrode, a first dielectric film and a first upper electrode,

the second capacitor element having a second lower electrode, a second dielectric film and a second upper electrode, and

the second dielectric film having a film thickness that is different from a film thickness of the first dielectric film.

2. A semiconductor device having a non-volatile memory transistor, comprising:

a first capacitor element and a second capacitor element,

the non-volatile memory transistor, the first and the second capacitor element being formed in one semiconductor substrate,

the capacitor element including a first lower electrode, a first dielectric film having a plurality of films as components and a first upper electrode,

the second capacitor element having a second lower electrode, a second dielectric film having a plurality of films as components and a second upper electrode, and

the components of the second dielectric film being different from the components of the first dielectric films.

3. A semiconductor device according to claim 1 or claim 2, wherein the first and the second dielectric film include an ONO film.

4. A semiconductor device according to claim 3, wherein

the first dielectric film has a structure including a thermal oxidation film, a nitride film and an oxide film successively laid in a direction from the first lower electrode toward the first upper electrode, and

the second dielectric film has a structure including a first thermal oxide film, a CVD oxide film, a second thermal oxide film, a nitride film and an oxide film successively laid in a direction from the second lower electrode toward the second upper electrode.

5. A semiconductor device according to claim 3, wherein

the first dielectric film has a structure including only a thermal oxidation film, a nitride film and an oxide film successively laid in a direction from the first lower electrode toward the first upper electrode, and

the second dielectric film has a structure including only a first thermal oxide film, a CVD oxide film, a second thermal oxide film, a nitride film and an oxide film successively laid in a direction from the second lower electrode toward the second upper electrode.

6. A semiconductor device according to claim 4, wherein

the thermal oxide film of the first dielectric film and the second thermal oxide film of the second dielectric film are formed in the same step,

the nitride film of the first dielectric film and the nitride film of the second dielectric film are formed in the same step, and

the oxide film of the first dielectric film and the oxide film of the second dielectric film are formed in the same step.

7. A semiconductor device according to claim 4, wherein the CVD oxide film of the second dielectric film includes a high-temperature CVD oxide film.

8. A semiconductor device according to claim 4, wherein each of the oxide film of the first dielectric film and the oxide film of the second dielectric film includes a thermal oxide film.

9. A semiconductor device according to claim 8, wherein

the thermal oxide film of the first dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 30 –200 angstrom,

the nitride film of the first dielectric film has a thickness of 50 – 500 angstrom,

the oxide film of the first dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 – 80 angstrom,

the first thermal oxide film of the second dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 – 80 angstrom,

the CVD oxide film of the second dielectric film has a thickness of 100 – 200 angstrom,

the second thermal oxide film of the second dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 30 – 200 angstrom,

the nitride film of the second dielectric film has a thickness of 50 –500 angstrom, and

the oxide film of the second dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 –80 angstrom.

10. A semiconductor device according to claim 4, wherein each of the oxide film of the first dielectric film and the oxide film of the second dielectric film includes a CVD oxide film.

11. A semiconductor device according to claim 10, wherein

the thermal oxide film of the first dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 30 –200 angstrom,

the nitride film of the first dielectric film has a thickness of 50 – 500 angstrom,

the oxide film of the first dielectric film has a thickness of 100 – 200 angstrom.

the first thermal oxide film of the second dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 – 80 angstrom,

the CVD oxide film of the second dielectric film has a thickness of 100 – 200 angstrom,

the second thermal oxide film of the another dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 30 – 200 angstrom,

the nitride film of the second dielectric film has a thickness of 50 –500 angstrom, and

the oxide film of the second dielectric film has a thickness of 100 –200 angstrom.

12. A semiconductor device according to claim 1 or claim 2, wherein the first and the second upper electrode are formed from polysilicon.

13. A semiconductor device according to claim 1 or claim 2, wherein the first and the second upper electrode are formed from polycide.

14. A semiconductor device according to claim 1 or claim 2, wherein the first and the second upper electrode are formed from metal.

15. A semiconductor device according to claim 1 or claim 2, wherein the first and the second upper electrode are formed from salicide.

16. A semiconductor device according to claim 1 or claim 2, wherein the first and the second lower electrode are films that are formed in the same step, and the first and the second upper electrode are films that are formed in the same step.

17. A semiconductor device according to claim 4, wherein the non-volatile memory transistor includes

a floating gate,

a control gate, and

an intermediate insulation film located between the floating gate and the control gate, wherein

the intermediate insulation film has a structure having a first thermal oxide film, a CVD oxide film, a second thermal oxide film and an oxide film that are successively disposed in a direction from the floating gate toward the control gate.

18. A semiconductor device according to claim 17, wherein

the first thermal oxide film of the intermediate insulation film and the first thermal oxide film of the second dielectric film are formed in the same step,

the CVD oxide film of the intermediate insulation film and the CVD oxide film of the second dielectric film are formed in the same step,

the second thermal oxide film of the intermediate insulation film, the thermal oxide film of the first dielectric film and the second thermal oxide film of the second dielectric film are formed in the same step, and

the oxide film of the intermediate insulation film, the oxide film of the first dielectric film and the oxide film of the second dielectric film are formed in the same step.

20. A semiconductor device according to claim 19, wherein the nitride film of the intermediate insulation film, the nitride film of the first dielectric film and the nitride film of the second dielectric film are formed in the same step.

22. A semiconductor device according to claim 17, wherein the oxide film of the intermediate insulation film includes at least one of a thermal oxide film and a CVD oxide film.

23. A semiconductor device according to claim 17, wherein the control gate, the first and the second upper electrode are formed from polysilicon.

24. A semiconductor device according to claim 17, wherein the control gate, the first and the second upper electrode are formed from polycide.

25. A semiconductor device according to claim 17, wherein the control gate, the first and the second upper electrode are formed from metal.

26. A semiconductor device according to claim 17, wherein the control gate, the first and the second upper electrode are formed from salicide.

27. A semiconductor device according to claim 17, wherein the floating gate, the first and the second lower electrode are formed in the same step, and

the control gate, the first and the second upper electrode are formed in the same step.

28. A semiconductor device according to claim 1 or claim 2, wherein an area of the first upper electrode that faces a surface of the first dielectric film is the same as an area of the second upper electrode that faces a surface of the second dielectric film.

29. A semiconductor device according to claim 1 or claim 2, wherein an area of the first upper electrode that faces a surface of the first dielectric film is different from an area of the second upper electrode that faces a surface of the second dielectric film.

30. A semiconductor device according to claim 1 or claim 2, wherein the second lower electrode has an impurity concentration different from an impurity concentration of the first lower electrode.

31. A semiconductor device according to claim 1 or claim 2, wherein the first dielectric film has a film thickness of 180 – 900 angstrom, and the second dielectric film has a film thickness of 340 – 1180 angstrom.

32. A semiconductor device according to claim 1 or claim 2, wherein the first capacitor element has a capacitor value that is different from a capacitor value of the second capacitor element.

33. A semiconductor device according to claim 1 or claim 2, wherein each of the first and the second capacitor element is a component of an analogue circuit.

35. A method for manufacturing a semiconductor device having a structure that includes a non-volatile memory transistor, a first and a second capacitor element formed in one semiconductor substrate, wherein the non-volatile memory transistor includes a floating gate, an intermediate insulation film and a control gate,

the first capacitor element includes a first lower electrode, a first dielectric film and a first upper electrode, and

the second capacitor element has a second lower electrode, a second dielectric film and a second upper electrode, the method comprising the steps of:

(a) forming the floating gate, the first and the second lower electrode on the semiconductor substrate;

(b) forming a first oxide film on the floating gate, the first and the second lower electrode;

(c) forming a second oxide film on the first oxide film;

(d) patterning the first oxide film and the second oxide film to thereby leave the first oxide film and the second oxide film that become components of the intermediate insulation film on sidewalls on the floating gate, to remove the first oxide film and the second oxide film on the first lower electrode, and to leave the first oxide film and the second oxide film that become components of the second dielectric film on the second lower electrode;

(e) forming a third oxide film that becomes a component of the intermediate insulation film, a component of the first dielectric film and a component of the second dielectric film on the second oxide film on the sidewall of the floating gate,

the first lower electrode and the second oxide film on the second lower electrode, respectively,

(f) forming a nitride film that becomes a component of the first dielectric film and a component of the second dielectric film on the third oxide film on the first lower electrode and the third oxide film on the second lower electrode, respectively,

(g) forming a fourth oxide film that becomes a component of the intermediate insulation film, a component of the first dielectric film and a component of the second dielectric film on the third oxide film on the sidewall of the floating gate, the nitride film on the first lower electrode and the nitride film on the second lower electrode, respectively, and

(h) forming, after the step (g), the control gate, the first and the second upper electrode on the semiconductor substrate.

36. A method for manufacturing a semiconductor device according to claim 35, wherein the step (a) includes the step of introducing an impurity in the first lower electrode to make the first lower electrode to have a first impurity concentration, and the step of introducing an impurity in the second lower electrode to make the second lower electrode to have a second impurity concentration that is different from the first impurity concentration.

44. A method for manufacturing a semiconductor device according to claim 35, wherein the step (f) includes the steps of:

forming a nitride film on the third oxide film;

forming a mask film on the nitride film on the third oxide film over the first lower electrode and on the nitride film on the third oxide film over the second lower electrode;

selectively removing the nitride film by anisotropic etching, using the mask film as a mask to leave the nitride film that becomes a component of the intermediate insulation film, a component of the first dielectric film and a component of the second dielectric film on the third oxide film on a sidewall lower

section of the floating gate, on the third oxide film on the first lower electrode and on the third oxide film on the second lower electrode, respectively.

48. A method for manufacturing a semiconductor device according to claim 35, wherein the step (a) includes the steps of:

forming a conductive film on the semiconductor substrate; and

patterning the conductive film to form the floating gate, the first and the second lower electrode at the same time.

49. A method for manufacturing a semiconductor device according to claim 35, wherein the step (h) includes the steps of:

forming another conductive film on the semiconductor substrate; and

patterning the another conductive film to form the control gate, the first upper electrode and the second upper electrode at the same time.